

## High Power DPDT Switch for GSM

### Description

The CXG1045N is a DPDT (Dual Pole Dual Throw) antenna switch MMIC used in personal communication handsets such as GSM, GSM1800 or dualband. This IC is designed using the Sony's GaAs J-FET process.

### Features

- Low insertion loss: 0.4dB (Typ.) @900MHz  
0.7dB (Typ.) @1.8GHz
- High power switching P1dB: 38dBm (Typ.) @900MHz  
37dBm (Typ.) @1.8GHz
- Small package SSOP-8pin: (3 × 6.4 × 1.25mm)
- Low current: 200μA (Typ.)

### Application

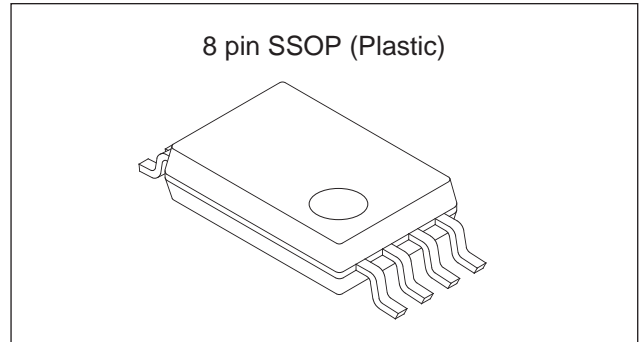
- GSM900 or GSM1800 handsets
- GSM900/GSM1800 dualband handsets

### Structure

GaAs J-FET MMIC

### Operating Condition

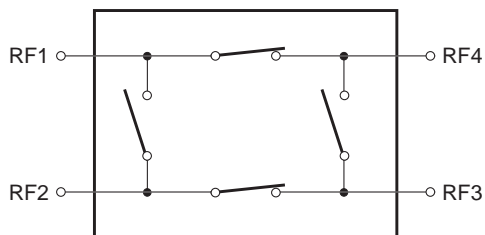
Control voltage:  $V_{ctl} (H) - V_{ctl} (L)$ : 2.5 to 5V @ $T_a = 25^\circ\text{C}$



\* GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Block Diagram



VCTLA	VCTLB	
High	Low	RF1 – RF2, RF3 – RF4 ON RF2 – RF3, RF4 – RF1 OFF
Low	High	RF1 – RF2, RF3 – RF4 OFF RF2 – RF3, RF4 – RF1 ON

Electrical Characteristics (1)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	*3, *4		0.4	0.7	dB
		*1, *2, *5		0.7	1.0	dB
Isolation	ISO	*3, *4	18	21		dB
		*1, *2, *5	15	17		dB
VSWR	VSWR	*1 to *5		1.2	1.4	
2nd harmonics	2fo	*1, *2			-31	dBm
		*3			-31	dBm
3rd harmonics	3fo	*1, *2			-31	dBm
		*3			-31	dBm
Input power for 1dB compression	P1dB	*3	36	38		dBm
		*1, *2	35	37		dBm
Switching time	TSW			100	500	ns
Control current	I CTL	0/5V control		200	350	μA

\*1 RF Input terminal is RF2. (RF2 → RF1, RF2 → RF3), Pin = 32dBm, 1710 to 1785MHz, 0/5V control

\*2 RF Input terminal is RF4. (RF4 → RF1, RF4 → RF3), Pin = 32dBm, 1710 to 1785MHz, 0/5V control

\*3 RF Input terminal is RF4. (RF4 → RF1, RF4 → RF3), Pin = 34.5dBm, 880 to 915MHz, 0/5V control

\*4 Pin = 10dBm, 925 to 960MHz, 0/5V control

\*5 Pin = 10dBm, 1805 to 1880MHz, 0/5V control

## Electrical Characteristics (2)

(Ta = -20 to +70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	*3, *4		0.4	1.0	dB
		*1, *2, *5		0.7	1.3	dB
Isolation	ISO	*3, *4	18	21		dB
		*1, *2, *5	15	17		dB
VSWR	VSWR	*1 to *5		1.2	1.4	
2nd harmonics	2fo	*1, *2			-31	dBm
		*3			-31	dBm
3rd harmonics	3fo	*1, *2			-31	dBm
		*3			-31	dBm
Input power for 1dB compression	P1dB	*3	36	38		dBm
		*1, *2	35	37		dBm
Switching time	TSW			100	500	ns
Control current	I CTL	0/5V control		200	400	μA

\*1 RF Input terminal is RF2. (RF2 → RF1, RF2 → RF3), Pin = 32dBm, 1710 to 1785MHz, 0/5V control

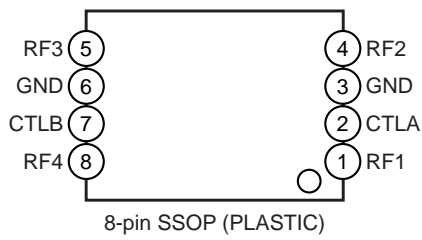
\*2 RF Input terminal is RF4. (RF4 → RF1, RF4 → RF3), Pin = 32dBm, 1710 to 1785MHz, 0/5V control

\*3 RF Input terminal is RF4. (RF4 → RF1, RF4 → RF3), Pin = 34.5dBm, 880 to 915MHz, 0/5V control

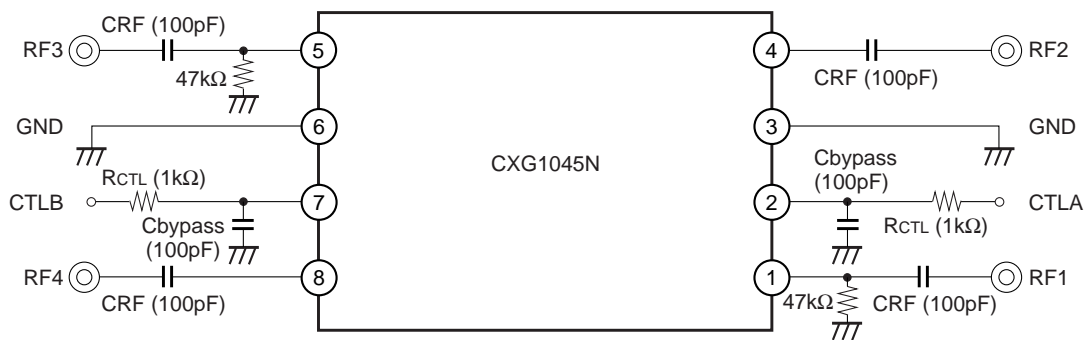
\*4 Pin = 10dBm, 925 to 960MHz, 0/5V control

\*5 Pin = 10dBm, 1805 to 1880MHz, 0/5V control

Package Outline/Pin Configuration



Recommended Circuit



- \* Recommended to use DC blocking capacitors (CRF) and bypass capacitors (Cbypass).
- \* Recommended to use control resistors (RCTL), when it is necessary to reduce the current consumption or to improve the electrostatic discharge (ESD) strength.

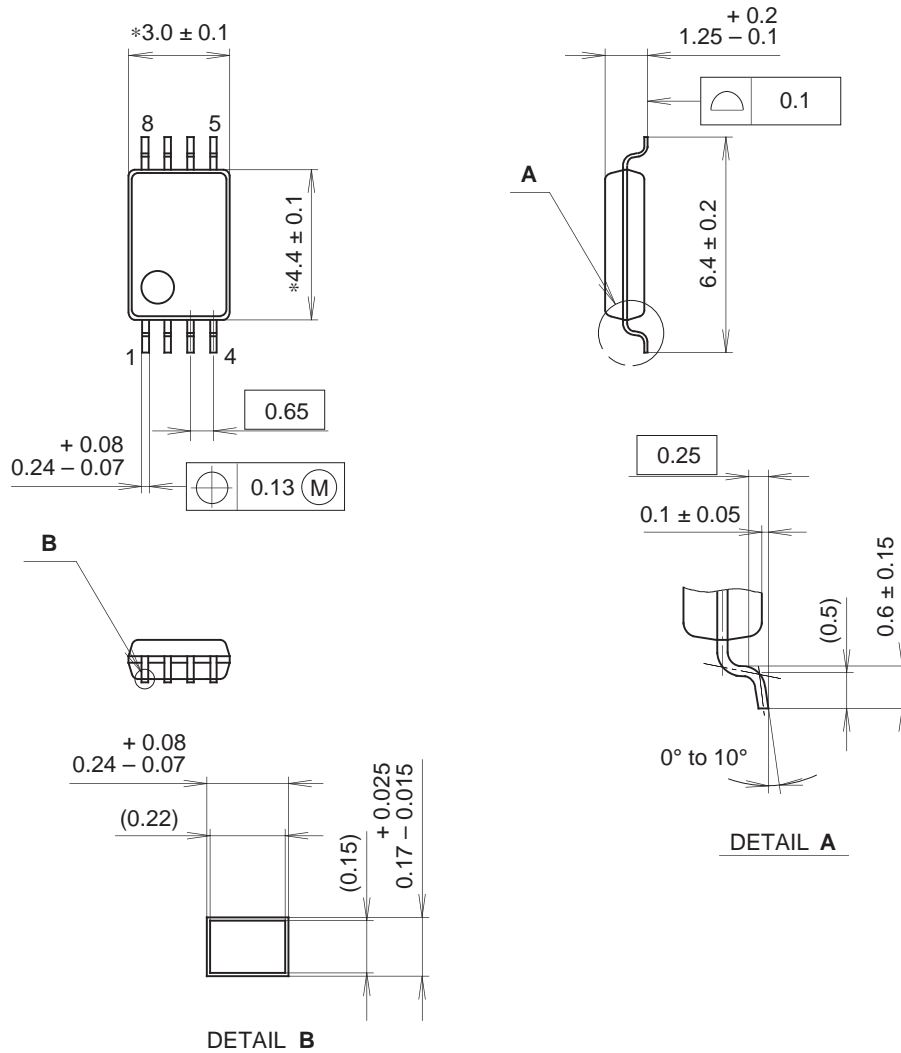
Absolute Maximum Ratings

- Control voltage      Vctl            7            V @Ta = 25°C
- Operating temperature    Topr        -35 to +85   °C
- Storage temperature      Tstg        -65 to +150   °C

Package Outline

Unit: mm

8PIN SSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-8P-L01
EIAJ CODE	SSOP008-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g